

Optimizing C Compiler and Instruction Scheduler

- Very Short Compile Times for Rapid Development
- Code Speed is Maximized by Optimization and An Advanced Instruction Scheduler Which Can Also Be Applied to Any Assembler Code
- Supports COFF-based Symbolic Debugging, and COFF to IEEE Translation
- Gives Original Source Code as Comments in Generated Assembler Code for Clarity
- Conforms to the ANSI C Standard (Verified with the Plum Hall Validation Suite)
- Includes Assembler, Linker, Librarian, and ROM Image Builder
- Unlimited Telephone Support with the Original Authors

Archelon C is a professional C package for the i960[®] microprocessor family. It includes an ANSI standard compiler, instruction scheduler, run-time library, assembler, linker, librarian, ROM image builder, and a driver program.

The instruction scheduler produces code that runs 20 percent faster by reorganizing instruction sequences to reduce pipeline stalls, and maximizing the throughput of the processor. The scheduler can work with either compiler-generated code or handwritten assembly code.

The compiler's optimizations are highly effective, and include global common subexpression elimination, automatic generation of leaf functions, automatic binding of variables, including small structures, to registers, constant folding, branch prediction, tail recursion elimination, and extensive peephole optimization.

The compiler can optionally interleave the original source text as comments among the generated assembly code.

The compiler is completely compatible with Intel's iC-960 C Compiler, supporting asm string insertion, asm function declaration, long double data type, align pragma, and iC-960 function calling conventions.

The compiler also supports GNU/960 alignment rules, interrupt functions, pseudo-variables for all registers, and a more convenient way of doing in-line assembly code.

Since it generates COFF symbolic debug tables, it works with any COFF symbolic debugger, such as Intel's DB960.

The DOS version requires an Intel386[™] processor or higher.

HOST SYSTEMS SUPPORTED:
MS-DOS PCs, SPARC, HPPA

PROCESSORS SUPPORTED:
i960 Processor Family

AVAILABILITY:
Now

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